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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,075	08/20/2004	Gary D. Grise	BUR920040061US1	5074

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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,075	GRISE ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2004*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-70* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-24, drawn to a method and a circuit for a control circuit **having a feedback connection**, classified in class 714, subclass 724.

   II. Claims 25-42, drawn to a method and a circuit for an integrated circuit which includes a test controller, **a clock splitter** and **an LSSD scan chain**, classified in class 714, subclass 731.

   III. Claims 43-58, drawn to a method and a circuit for an integrated circuit which includes a test controller and a scan chain having serially connected latches and corresponding **multiplexers**, classified in class 714, subclass 726.

   IV. Claims 59-70, drawn to a method and a circuit for an integrated circuit which includes a test controller and a scan chain having serially connected latches and corresponding **de-multiplexers**, classified in class 714, subclass 726.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions I, II, III and IV are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for

patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). The instant case is as follow:

a. Invention I has separate utility such as **a control circuit** that comprises an output of a first latch connected to an input of a second latch, an output of said second latch connected to an input of a third latch, said second latch **having a feedback connection** to an input of said first latch and said third latch having feedback connections to said first and said second latches, **combinational logic** coupled to said first, second and third latches, said combinational logic having a test signal input, a test clock input and a functional clock input, said feedback connection of said second latch further coupled through said combinational logic to a first control signal output and said first latch coupled through said combinational logic to a second control signal output. These are patentably distinct features not found in inventions II, III and IV.

b. Invention II has separate utility such as an integrated circuit that comprises a test pin, a first test clock pin, a second test clock pin, a third test clock pin a functional clock pin, a scan-in pin, a scan-out pin and an enable pin **a test controller** having a test input connected to said test pin, a first test clock input connected to said first test clock pin, a functional clock input connected to said functional clock pin, a first control output and a second control output, **a clock splitter** having a first clock input connected to said second test clock pin, a second clock input connected to said functional clock pin, a first control input connected to said first control output of said test controller, a second control input

connected to said second control output and of said controller, an enable input connected to said enable pin, a ZB clock output and a ZC clock output and **an LSSD scan chain** comprised of serially connected latches, a first stage of each latch having an first data input, a second data input and a C clock input connected to said ZC clock output of said clock splitter, an A CLK input connected to said third test clock pin, a second stage of each latch having a data output and a B clock input connected to said ZB clock output of said clock splitter, a data output of a previous latch connected to a first input pin of an immediately subsequent latch, a first data input of a first latch of said LSSD scan chain connected to said scan-in pin and a data output pin of a last scan chain latch of said scan chain connected to said scan-out pin. These are patentably distinct features not found in inventions I, III and IV.

c. Invention III has separate utility such as an integrated circuit that comprises a test pin, a select enable pin, a functional clock pin, a scan-in pin and a scan-out pin (**This is a different input-output pin configuration than the integrated circuit of Invention II above**), **a test controller** having a test input connected to said test pin, a functional clock input connected to said functional clock pin, a first control output and a second control output (**This is a different test controller than test controller of Invention II or IV**), **a scan chain** comprised of serially connected latches and **corresponding multiplexers**, a first stage of each latch having a data input, a clock input connected to a functional clock pin, a first control input connected to said first control output of said test

controller, a second stage of each latch having a data output and a second control input connected to said second control output of said tester controller, a data output of a previous latch connected to a first selectable input of a multiplexer corresponding to an immediately subsequent latch, a selected output of said corresponding multiplexer connected to said data input of said immediately subsequent latch, a first selectable data input of a multiplexer of said scan chain connected to said scan-in pin and a data output of a last latch of said scan chain connected to said scan-out pin. These are patentably distinct features not found in inventions I, II and IV.

d. Invention IV has separate utility such as an integrated circuit that comprises a test pin, a select enable pin, a functional clock pin, a scan-in pin and a scan-out pin, **a test controller** having a test input connected to said test pin, a select enable input connected to said select enable pin, a functional clock input connected to said functional clock pin, and a control output (**This is a different test controller than test controller of Invention II or III**), **a scan chain** comprised of serially connected latches and **corresponding de-multiplexers**, a first stage of each latch having a data input and a clock input connected to a functional clock pin, a second stage of each latch having a data output, a data output of a previous latch connected to a first selectable input of a multiplexer corresponding to an immediately subsequent latch, a selected output of said corresponding multiplexer connected to said data input of said immediately subsequent latch, a first selectable data input of a multiplexer of said scan chain

connected to said scan-in pin and a selected output of a last latch of said scan chain connected to said scan-out pin and each multiplexer of said scan chain having a select input connected to said control output of said test controller. The **test controller** and composition of the scan chain using **de-multiplexers** are patentably distinct features not found in inventions I, II and III.

3. The examiner has required restriction between combination and subcombination inventions. Where applicants elect a subcombination, and claims thereto are subsequently found allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicants are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

4. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

5. Applicants are reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

6. Applicants are advised that the reply to this requirement to be complete must include (i) an election of a species or invention to be examined even though the requirement be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

7. In order to expedite the prosecution for the subject application, **the non-elected claims should be canceled in response to this office action**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr. 9/28/06
John J. Tabone, Jr.
Examiner
Art Unit 2138

CHRISTINE T. TU
Primary Examiner